# POWER TRANSISTOR AND SEMICONDUCTOR INTEGRATED CIRCUIT USING THE SAME

## BACKGROUND OF THE INVENTION

**[0001]** The present invention relates to a power transistor and a semiconductor integrated circuit using the same. More particularly, the invention relates to a power transistor, as well as a semiconductor integrated circuit using the same, in which a plurality of vertical PNP transistors are arrayed.

**[0002]** Conventionally, there has been provided a power transistor in which a plurality of vertical PNP transistors are arrayed on a semiconductor substrate (see, for example, Japanese Patent Laid-Open Publication HEI 7-183311).

**[0003]** Fig. 3 shows a pattern plan view of a conventional power transistor, and Fig. 4 shows a sectional view taken along the line IV-IV of Fig. 3. In this power transistor, there are formed, on a P-type silicon substrate 101: an $N^+$ type buried layer 102 for isolating the P-type silicon substrate 101 and a collector of each vertical PNP transistor from each other; a $P^+$ type collector buried layer 103 which is formed on the $N^+$ type buried layer 102 and which serves as the collector of each vertical PNP transistor; a $P^+$ type buried isolation layer 113 formed around the $N^+$ type buried layer 102 to isolate the power

transistor and its peripheral devices from each other; an N-type epitaxial layer 104 formed all over the surface of the P-type silicon substrate 101 by N-type epitaxial growth; an $N^+$ type base well layer 105 formed as a base region of each vertical PNP transistor to improve the transistor characteristics; a $P^+$ type collector layer 106 formed on the $P^+$ type collector buried layer 103; a $P^+$ type isolation layer 116 formed at an upper portion of the $P^+$ type buried isolation layer 113 serving for device isolation; a $P^+$ type emitter layer 107 serving as an emitter of each vertical PNP transistor formed within the region of the $N^+$ type base well layer 105; an $N^+$ type base layer 108 formed in the base electrode region of each vertical PNP transistor; and an $N^+$ type electrode layer 118 which is formed so as to surround the $P^+$ type collector layer 106 for taking the electrode of the $N^+$ type buried layer 102 located just under the power transistor region. Also, a selectively patterned and opened oxide film 120 is formed on the surface of the P-type silicon substrate 101, and further thereon are formed common emitter metal lines 109, common base metal lines 110 and common collector metal lines 111 routed for electrical connections among a plurality of unit transistors constituting the power transistor, as well as metal lines 112 of the $N^+$ type buried layer 102 connected to the common emitter metal

lines 109 and grounded to GND. It is noted that all of these are formed by a known standard bipolar IC manufacturing method. In Fig. 3, since the common base metal lines 110 are of less importance for the present invention, their interconnect lines are partly omitted.

**[0004]** With the structure of this conventional power transistor, there has been a problem that with the vertical PNP transistors in the saturation region, the parasitic PNP transistor would malfunction, causing leak currents to flow to the P-type silicon substrate, so that the voltage level of the P-type silicon substrate would be unstable, causing latch-up of peripheral circuits of the power transistor, which would lead to circuit malfunctions. The mechanism of occurrence of leak currents with the vertical PNP transistors in the saturation region is explained below by using part of the cross-sectional structure of the power transistor.

**[0005]** Fig. 5 is a sectional view of the power transistor with the vertical PNP transistors in the saturation region, where while the vertical PNP transistors are in the saturation region, the common emitter metal lines 109 and the metal lines 112 of the $N^+$ type buried layer 102 routed and connected with the common emitter metal lines 109 are given a voltage of 0 V, the common base metal lines 110 are given a voltage of -0.6 V, and the

common collector metal lines 111 are given a voltage of -0.3 V. It is noted that in Fig. 5, solid-line arrows represent holes and broken-line arrows represent electrons.

**[0006]** First, as an input current of the vertical PNP transistors, holes are injected from the $P^+$ type emitter layer 107 into the $N^+$ type base well layer 105, making a base current flow (represented by solid-line arrow A in Fig. 5). With the vertical PNP transistors in the saturation region, the $P^+$ type collector buried layer 103 and the $N^+$ type base well layer 105 have a forward bias of 0.3 V applied therebetween, so that electrons are injected from the $N^+$ type base well layer 105 to the $P^+$ type collector buried layer 103 (represented by broken-line arrow B in Fig. 5).

**[0007]** Then, part of the injected electrons reach up to the $N^+$ type buried layer 102, where those are recombined and dissipated (broken-line arrow C in Fig. 5). In this case, since the $N^+$ type buried layer 102 are routed and connected to the common emitter metal lines 109 and grounded to GND by the metal lines 112 via its own resistance R1 and the resistance R2 of the N-type epitaxial layer 104, the large values of the resistance R1 and resistance R2 would cause part of the injected electrons to return to the $P^+$ type collector buried layer 103 without recombining (broken-line arrow C' in Fig. 5).

**[0008]** By the electrons that have returned to the $P^+$ type collector buried layer 103 without recombining, holes are injected from the $P^+$ type collector buried layer 103 into the $N^+$ type buried layer 102 (solid-line arrow D in Fig. 5). With causing the voltage of the $N^+$ type buried layer 102 to lower, a hole current is hFE-multiplied by the parasitic PNP transistor (a transistor comprised of the $P^+$ type collector buried layer 103 as an emitter, the $N^+$ type buried layer 102 as a base and the P-type silicon substrate 101 as a collector), thus flowing as a leak current through the P-type silicon substrate 101 (solid-line arrow E in Fig. 5).

**[0009]** In this conventional power transistor, as shown in Fig. 4, since electrode portions of the $N^+$ type buried layer 102 (pattern region of the $N^+$ type electrode layer 118) are provided so as to surround the active region of the power transistor, the distance from the $N^+$ type buried layer 102 just under central portion of the power transistor to the electrode portion becomes a long one so that the resistance R1 becomes very large. Thus, there has been a problem that with the power transistor in the saturation region, the parasitic PNP transistor would be more likely to malfunction, causing a leak current to flow to the P-type silicon substrate 101.

[0010] These problems are critical problems that could resultantly cause voltage level of the P-type silicon substrate 101 unstable, leading to occurrence of latch-up of peripheral circuits of the power transistor, and thus to circuit malfunctions.

SUMMARY OF THE INVENTION

[0011] Accordingly, an object of the present invention is to provide a power transistor, as well as a semiconductor integrated circuit using the power transistor, in which malfunctions of the parasitic PNP transistor of the power transistor are suppressed so that circuit malfunctions due to latch-up of the peripheral circuits are prevented.

[0012] In order to achieve the above object, according to the present invention, there is provided a power transistor composed of a plurality of vertical PNP transistors formed on a P-type silicon substrate, wherein

a singularity or plurality of electrode portions of an $N^+$ type buried layer formed to isolate the P-type silicon substrate and the plurality of vertical PNP transistors from each other are provided in an active region of the power transistor.

[0013] In this power transistor, by the provision of one or more electrode portions of the $N^+$ type buried layer

within the power-transistor active region, the distance from the $N^+$ type buried layer just under the power transistor to the electrode portions becomes shorter, and so the resistance thereof becomes smaller. Thus, malfunctions of the parasitic PNP transistors can be prevented, and circuit malfunctions due to latch-up of the peripheral circuits of the power transistor can be prevented.

**[0014]** In one embodiment, at least part of the electrode portion is provided under common emitter metal lines of the power transistor routed on the active region of the power transistor.

**[0015]** In the power transistor of this embodiment, by the provision of the electrode portions of the $N^+$ type buried layer under the common emitter metal lines of the power transistor formed and routed on the power-transistor active region, effective use of the limited design space of the power transistor can be made without increasing the power transistor size, thus making it unnecessary to make complex pattern design.

**[0016]** Also, in one embodiment, the electrode portions are provided on the $N^+$ type buried layer and formed of an $N^+$ type electrode layer for making ohmic contact and an $N^+$ type diffusion layer.

[0017] Whereas the primary cause of malfunctions of the parasitic PNP transistors is that the resistance component of the $N^+$ type buried layer is large, the resistance of the N-type epitaxial layer present longitudinally from the $N^+$ type electrode layer to the $N^+$ type buried layer provided at the bottom face of the power transistor is another cause, which is less influential as it is. Thus, according to the power transistor of this embodiment, an $N^+$ type diffusion layer heavier in dopant level than the N-type epitaxial layer is formed at the electrode portions of the $N^+$ type buried layer, by which the resistance of up to the $N^+$ type buried layer can be reduced, so that malfunctions of the parasitic PNP transistors can be prevented.

[0018] Also, in one embodiment, the $N^+$ type diffusion layer is formed simultaneously with an $N^+$ type base well layer as a base region of the plurality of vertical PNP transistors.

[0019] In the power transistor of this embodiment, the $N^+$ type base well layer, which is needed for characteristic improvement of the vertical PNP transistors and formed over the base region of the vertical PNP transistors, and the $N^+$ type diffusion layer are formed simultaneously. Thus, it becomes possible to lessen the resistance of the N-type epitaxial layer without involving any additional process.

**[0020]** Also, in one embodiment, the $N^+$ type diffusion layer is formed at a range of dopant level of $1\times10^{16}$ to $1\times10^{17}$ atoms/$cm^3$, which is heavier than that of an N-type epitaxial layer formed on the P-type silicon substrate.

**[0021]** In the power transistor of this embodiment, the practical-use range of dopant level of the $N^+$ type diffusion layer is set heavier than that of the N-type epitaxial layer and such light as not to affect the characteristic of the vertical PNP transistors. In consideration of this, the practical-use range of dopant level is preferably $1\times10^{16}$ to $1\times10^{17}$ atoms/$cm^3$. As a result of this, the longitudinally-present resistance of the N-type epitaxial layer can be reduced.

**[0022]** Also, in one embodiment, the $N^+$ type diffusion layer is formed so that dopants are diffused until they reach the $N^+$ type buried layer present on a bottom face of the power transistor.

**[0023]** In the power transistor of this embodiment, the $N^+$ type diffusion layer is formed so as to be diffused until it reaches the $N^+$ type buried layer provided at the bottom face of the power transistor. Thus, the resistance of the N-type epitaxial layer can be reduced, and it never occurs that the resistance increases while the N-type epitaxial layer remains.

[0024] Also, in one embodiment, the singularity or plurality of electrode portions are placed so as to be uniformly spaced from their respectively adjacent electrode portions.

[0025] In the power transistor of this embodiment, a plurality of electrode portions are placed so as to be uniform in distance to their respectively adjacent electrode portions of the $N^+$ type buried layer, so that the resistance of the $N^+$ type buried layer just under the power-transistor active region can be made smaller, so that the resistance distribution of the buried layer can be uniformized, thus making it possible to suppress the occurrence of local leak currents. Further, although depending on the resistance value of the $N^+$ type buried layer, hFE of the parasitic PNP transistors, and the like, the number of placed electrode portions of the N+ type buried layer, if required, can be increased to reduce the resistance.

[0026] Furthermore, according to the present invention, there is provided a semiconductor integrated circuit which uses any one of the power transistors as described above.

[0027] In this semiconductor integrated circuit, a power transistor that can be prevented from malfunctions of the parasitic PNP transistors and circuit malfunctions due to latch-up of the peripheral circuits is used. Thus, there

can be provided a high-performance semiconductor integrated circuit capable of stable operation.

## BRIEF DESCRIPTION OF THE DRAWINGS

**[0028]** The present invention will become more fully understood from the detailed description given hereinbelow and the accompanying drawings which are given by way of illustration only, and thus are not limitative of the present invention, and wherein:

**[0029]** Fig. 1 is a plan view of a power transistor according to an embodiment of the present invention;

**[0030]** Fig. 2 is a sectional view taken along the line II - II of Fig. 1;

**[0031]** Fig. 3 is a pattern plan view of a power transistor according to a prior art;

**[0032]** Fig. 4 is a sectional view taken along the line IV - IV of Fig. 3; and

**[0033]** Fig. 5 is a view showing the cross-sectional structure of the vertical PNP transistor in the saturation region.

## DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

**[0034]** Hereinbelow, the power transistor of the present invention is described in detail by way of embodiments thereof illustrated in the accompanying drawings.

**[0035]** Fig. 1 is a pattern plan view of a power transistor according to an embodiment of the present invention, and Fig. 2 is a sectional view taken along the line II - II of Fig. 1.

**[0036]** In this power transistor, as shown in Figs. 1 and 2, there are formed, on a P-type silicon substrate 1: an $N^+$ type buried layer 2 for isolating the P-type silicon substrate 1 and a collector of each vertical PNP transistor from each other; a $P^+$ type collector buried layer 3 which serves as the collector of each vertical PNP transistor; a $P^+$ type buried isolation layer 13 formed around the $N^+$ type buried layer 2 to isolate the power transistor and its peripheral devices from each other; a an N-type epitaxial layer 4 formed all over the surface of the P-type silicon substrate 1 by epitaxial growth; an $N^+$ type base well layer 5 formed at a base region of each vertical PNP transistor to improve the transistor characteristics; an $N^+$ type diffusion layer 15 formed at electrode portions 'a' of the $N^+$ type buried layer 2 (just under an $N^+$ type electrode layer 18) which are conventionally formed so as to surround the power transistor, as well as at electrode portions 'a' of an $N^+$ type buried layer 2 within the active region of the power transistor in order to reduce the resistance of the N-type epitaxial layer 4; a $P^+$ type collector layer 6 formed on the $P^+$ type collector buried layer 3; a $P^+$ type

isolation layer 16 formed on the $P^+$ type buried isolation layer 13 serving for device isolation; a $P^+$ type emitter layer 7 serving as an emitter of each vertical PNP transistor formed within the region of the $N^+$ type base well layer 5; and an $N^+$ type base layer 8 formed in the base electrode region of each vertical PNP transistor.

**[0037]** Also, a selectively patterned and opened oxide film 20 is formed on the surface of the P-type silicon substrate 1, and further thereon are formed common emitter metal lines 9, common base metal lines 10 and common collector metal lines 11 which are routed for electrical connections among a plurality of unit transistors constituting the power transistor, as well as metal lines 12 of the $N^+$ type buried layer 2 electrically connected to the common emitter metal lines 9 and grounded to GND. That is to say, the common emitter metal lines 9 are electrically connected to the metal lines 12, though not shown in Fig. 2.

**[0038]** It is noted that the electrode portions 'a' of the $N^+$ type buried layer 2 formed within the active region of the power transistor are connected by the common emitter metal lines 9. This electrode portions 'a' are composed of the $N^+$ type diffusion layer 15 and $N^+$ type electrode layers 18 under the common emitter metal lines 9. The $N^+$ type electrode layer 18 and the common emitter metal line 9 make

ohmic contact. The power transistor of this invention is formed by a known standard bipolar IC manufacturing method. In Fig. 1, since the common base metal lines 10 are of less importance for the present invention, their interconnect lines are partly omitted.

**[0039]** With the power transistor of this construction, malfunctions of the parasitic PNP transistor, which have hitherto been an issue, can be prevented so that the leak current to the P-type silicon substrate 1 can be suppressed, and thus circuit malfunctions due to latch-up of the peripheral circuits of the power transistor can be prevented.

**[0040]** By experiments performed by the present inventor, it has been verified that the leak current of the power transistor designed based on this embodiment of the invention is improved to about 20%, compared to the conventional counterpart.

**[0041]** The plurality of electrode portions 'a' of the $N^+$ type buried layer 2, which need to be equal in voltage level to the common emitter metal lines 9 of the power transistor, can be connected directly to the common emitter metal lines 9 formed and routed on the active region of the power transistor, effective use of the limited design space of the power transistor can be made, making it unnecessary to make complex pattern design.

**[0042]** Also, the $N^+$ type diffusion layer 15 of the electrode portions 'a' of the $N^+$ type buried layer 2 are formed simultaneously with the $N^+$ type base well layer 5, so that dopants are diffused and formed at a dopant concentration level heavier than that of the N-type epitaxial layer 4 and until they reach the lower-portion $N^+$ type buried layer 2. As a result of this, it becomes possible to reduce the resistance R2 ranging from the $N^+$ type electrode layer 18 to the $N^+$ type buried layer 2 provided at the bottom face of the power transistor.

**[0043]** Typically, the N-type epitaxial layer of a bipolar IC (Integrated Circuit) is formed generally at a specific resistance of 1 to 5 Ω·cm (dopant level: 1 to $5\times10^{15}$ atoms/$cm^3$). However, in consideration of the $N^+$ type base well layer 5 that affects the characteristics of vertical PNP transistors, it is desirable that the $N^+$ type diffusion layer 15 is formed at a dopant level within a range of $1\times10^{16}$ to $1\times10^{17}$ atoms/$cm^3$.

**[0044]** Also, the electrode portions 'a' of the $N^+$ type buried layer 2 (region of the $N^+$ type electrode layer 18), which are conventionally formed around the power-transistor active region, and the plurality of electrode portions 'a' of the N+ type buried layer 2 provided within the active region, are placed so as to be spaced at shorter distances therebetween and arranged uniformly. As a result of this,

the resistance R1 of the $N^+$ type buried layer 2 just under the power transistor can be made smaller, and the resistance distribution of the $N^+$ type buried layer 2 can be uniformized, thus making it possible to suppress the occurrence of local leak currents.

**[0045]** Further, although depending on the resistance value of the $N^+$ type buried layer 2, hFE of the parasitic PNP transistors, and the like, the number of placed electrode portions 'a' of the N+ type buried layer 2, if required, can be increased to reduce the resistance R1.

**[0046]** Although the above embodiment has been described on a power transistor in which a plurality of vertical PNP transistors are formed on the P-type silicon substrate 1, the semiconductor substrate is not limited to silicon substrates and may be those made of other materials. Further, although the above embodiment has been described on a power transistor in which a plurality of electrode portions 'a' of the N+ type buried layer 2 are provided, yet the electrode portion 'a' may be given one in number, and the placement or number of the electrode portions 'a' may be set as required according to the construction of the vertical PNP transistors or the like.

**[0047]** Furthermore, using the power transistor of the above embodiment for integrated circuits makes it possible

to implement a high-performance integrated circuit capable of stable operation.

**[0048]** As apparent from the above description, according to the power transistor of the present invention, by the provision of a plurality of electrode portions of the $N^+$ type buried layer within the power-transistor active region, resistance over a range from the $N^+$ type buried layer to the electrode layer can be reduced, so that malfunctions of the parasitic PNP transistors can be prevented, making it possible to suppress the leak currents to the P-type silicon substrate. Thus, circuit malfunctions due to latch-up of the peripheral circuits of the power transistor can be prevented.

**[0049]** Further, according to the semiconductor integrated circuit of the present invention, by using the above-described power transistor, a high-performance semiconductor integrated circuit capable of stable operation can be provided.

**[0050]** The invention being thus described, it will be obvious that the same may be varied in many ways. Such variations are not to be regarded as a departure from the spirit and scope of the invention, and all such modifications as would be obvious to one skilled in the art are intended to be included within the scope of the following claims.